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10/631,098	07/31/2003	Steven H. Voldman	BUR9-1999-0193US2	7752

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,098	VOLDMAN, STEVEN H.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14,15,17-20,22 and 24-36* is/are pending in the application.

4a) Of the above claim(s) *15,19,20 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14,17,18 and 24-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 14, 17, 18 and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al. (USP 5,528,188) in view of Brady et al. (USP 5,314,841).

With respect to claims 14 and 17, Figure 4b of the Au et al. reference discloses a device which includes: a MOSFET transistor (Q1) comprising a gate (gate of Q1), a body (body of Q1); an RC discriminator circuit (32) comprising a resistor (R) and a capacitor (C), and a circuit control network (40) modulating a potential of the body (of M) to provide ESD protection (the circuit of 40 capable of controlling the potential biasing the body of the transistor and therefore it also capable of provide ESD protection) . The Au et al. reference does not disclose that the MOSFET Q1 in Figure 4b is fabricated by using silicon-over-insulator SOI technology. However, the Brady et al. reference discloses that silicon-over-insulator (SOI) technology provides advantages over regular silicon technology such as increasing the operating speed and reducing the power consumption of the circuitry (Col. 1, lines 12-15). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the circuit in Figure 4b of the Au et al. reference by using specific SOI technology to fabricate the MOSFET transistor for the purpose of increasing the operating speed and reducing the power consumption of the circuitry. Thus, this modification meets all the limitation of

claims 14 and 17. Note that, in this modification, "the body that is floating with respect to an underlying substrate" on line 3 of claim 14 is met when fabricate the device by using SOI technology (i.e., the body of Q1, Figure 4b in the above modification is floating with respect to an underlying substrate) because the body of an SOI MOSFET is floating with respect to an underlying substrate. Also, note that, the functional limitation in claim 17 is also met as the operation of control network circuitry modulates the potential voltage of the body and limit the body to a reference voltage.

With respect to claims 31 and 32, the modification/combination of Au et al. and Brady et al. as discussed in claim 14 above meets all the limitations of this claim except that the resistor R is a resistive-transistor. However, it is art-recognized that a resistor could be easily implemented in an integrated circuitry by using a transistor that has its gate connected to DC bias so that the transistor is in an ON state (evidence is shown in the Sasaki reference, USP 5,039,873, that a MOSFET transistor is functionally equivalent to a resistor when the MOSFET transistor is ON, see Figure 4c, and Col. 1, lines 21-22 of Sasaki). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the above circuitry by substitute an always ON MOSFET transistor (i.e., a MOSFET transistor having a DC bias at its gate so that the MOSFET transistor is ON) for each of the resistors in the circuitry because they are functionally equivalent and for the purpose that it is easily integrated. With such a modification, the limitation of claim 31 is met as that the RC discriminator including a resistive-transistor and a capacitor (also note that because the circuitry is fabricated by using SOI technology as discussed in claim 14, so the body of the SOI transistor is floating with respect to an underlying substrate). Note that, in the above modification, the functional limitation in claim

32 is also met as the operation of control network circuitry modulates the potential voltage of the body and limit the body to a reference voltage. Also, note that the device includes a source S and a drain D (Figure 4b of Au et al.), wherein the source is connected to the resistive-transistor (both connected to ground), and the drain is connected to the capacitor as recited in claim 34; and the functional limitation that the resistive transistor and said capacitor initiate coupling of the gate when an over-voltage or over-current condition exits (recited in claim 35) is also met (Col. 5, lines 30-67 of Au et al.) and also because the structure of the RC discriminator connected to the gate of the MOSFET device of the Au et al. is substantially identical as the structure of the RC discriminator of the inventions. Also, Figure 4b of the Au et al. shows a PAD (PAD) coupled to the capacitor (for claim 36).

With respect to claims 18 and 33, the modification/combination as discussed in claim 31 meets the limitations of these claims that the circuit control network (40, Figure 4b of Au et al.) includes at least a SOI MOSFET because the circuitry is fabricate by using SOI technology (discussed in claim 14), and because every resistor in the circuitry is formed by using an always ON MOSFET transistor (as discussed in claim 31) so the SOI MOSFET in this claim is the always ON MOSFET transistors for resistors R1 and R2 in circuit 40 of Figure 4b.

3. Claims 24 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (USP 5,631,793) in view of Au et al. (USP 5,528,188), and further in view of Brady et al. (USP 5,314,841).

With respect to claim 24, Figure 2 of the Ker reference discloses a device which includes: an n-channel MOSFET (Mn1) comprising a first body and a first gate; a p-channel MOSFET (Mp1) comprising a second body and a second age; a first RC discriminator (Rn, Cn1)

comprising a first resistor (Rn) and a first capacitor (Cn1); and a second RC discriminator (Rp , Cp1) comprising a second resistor (Rp) and a second capacitor (Cp1). The Ker reference does not discloses the device a first circuit control network for modulating a potential voltage of the first body, and a second circuit control network for modulating a potential voltage of the second body. However, the Au et al. reference discloses in Figure 6 a device that includes first and second circuit control networks (SCR 52 and 50, wherein the detail of the SCR is shown as circuit 40 in Figure 4b) for controlling the first and second bodies (bodies of Q3 and Q2), respectively for the purpose of improving the level of ESD protection of either a positive or negative polarity ESD event (see line 59 of Col. 5 to line 23 of Col. 6). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to provide the device of Figure 2 of the Ker et al. reference with the first and second circuit control networks connected to the first and second bodies, respectively, for the purpose of improving the level of ESD protection of either a positive or negative polarity ESD event. Thus, this modification meets the limitations of the first and second circuit control networks as recited in claim 24 including the functional limitation "to provide ESD protection".

The combination of the Ker et al. reference and the Au et al. reference meets all the limitations of claim 24 except that the circuitry is fabricated by using silicon-over-insulator SOI technology. However, the Brady et al. reference discloses that silicon-over-insulator (SOI) technology provides advantages over regular silicon technology such as increasing the operating speed and reducing the power consumption of the circuitry (Col. 1, lines 12-15 of Brady et al.). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify above combination by using specific SOI technology to fabricate

the circuitry for the purpose of increasing the operating speed and reducing the power consumption of the circuitry. Thus, this modification meets all the limitation of claim 24. Note that, in this modification, "a fist body that is floating with respect to an underlying substrate" on line 3-4 and "a second body that is floating with respect to said underlying substrate" on line 6-7 of claim 14 is met when fabricate the device by using SOI technology (i.e., the bodies of Mp1 and Mn1, Figure 2 of Ker et al. in the modification are floating with respect to the underlying substrate) because the body of an SOI MOSFET is floating with respect to an underlying substrate

With respect to claim 26, Figure 2 of the Ker et al. in the above combination shows the n-channel SOI MOSFET Mn1 comprises a source and a drain connected to the first resistor (Rn) and the first capacitor (Cn1); and the p-channel SOI MOSFET transistor includes a source and a drain connected to the second resistor (Rp) and the second capacitor (Cp1).

With respect to claim 27, the functional limitation that the first resistor and capacitor and the second resistor and capacitor initiate coupling of the first gate and the second gate, respectively, when an over-voltage or over-current condition exists is met (see line 65 of Col. 4 to line 5 of Col. 5). Further, because the structure of the first and second RC discriminator circuit connected to the first and second gates is substantially identical to applicant's invention so it must functions the same.

With respect to claim 28, it is seen in the operation of the combination/modification circuitry that the first circuit control network limits the first body to a reference voltage, and the second circuit control network limits the second body to the reference voltage (both of the circuit

control networks SCR in the above combination/modification are the same so they must limit the same reference voltage).

With respect to claim 29, it is seen that the two circuit control networks SCR in the above combination/modification coupled to difference voltages, i.e., the one that is coupled to the body of the p-channel MOSFET is coupled to the power supply voltage, and the one that is coupled to the body of the n-channel MOSFET is coupled to ground.

With respect to claim 30, the above combination/modification circuitry shows a pad (21, Figure 2 of Ker et al.) connected between the n-channel and p-channel SOI MOSFETs.

4. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (USP 5,631,793) in view of Au et al. (USP 5,528,188) and Brady et al. (USP 5,314,841).

With respect to claim 25, the modification/combination of Ker et al., Au et al. and Brady et al. as discussed in claim 24 above meets all the limitations of this claim except that first and second circuit control network comprises at least one SOI MOSFET. However, it is art-recognized that a resistor could be easily implemented in an integrated circuitry by using a transistor that has its gate connected to DC bias so that the transistor is in an ON state (evidence is shown in the Sasaki reference, USP 5,039,873, that a MOSFET transistor is functionally equivalent to a resistor when the MOSFET transistor is ON, see Figure 4c, and Col. 1, lines 21-22 of Sasaki). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the above combination/modification circuitry by substitute an always ON MOSFET transistor (i.e., a MOSFET transistor having a DC bias at its gate so that the MOSFET transistor is ON) for each of the resistors in the circuitry because they are functionally equivalent and for the purpose that it is easily integrated. With this

modification, the limitations of this claim is met because the first and second circuit control networks (40, Figure 4b of Au et al.) includes at least a SOI MOSFET because the circuitry is fabricate by using SOI technology, and because every resistor in the circuitry is formed by using an always ON MOSFET transistor so the SOI MOSFET in this claim is the always ON MOSFET transistors (for resistors R1 and R2 in circuit 40 of Figure 4b of Au et al.).

Response to Arguments

5. Applicant's arguments filed 09/08/05 have been fully considered but they are not persuasive.

Applicant argues that the circuitry within Au cannot be constructed in SOI because the SCR cannot be built in SOI since there is no N-well in SOI technology. However, this argument is not persuasive because the MOSFET Q1, Figure 4b in Au is properly be constructed in SOI technology and when fabricate in SOI technology, the body of Q1 is floating with respect to an underlying substrate, and the body of Q1 is controlled by the control network 40, and note that the floating of body Q1 does not effect the operating of the SCR control network 40.

Applicant also argues that "as shown in Figure 4b of Au, a network exists between the pad 34 and ground potential. To the contrary, with the claimed invention, because of the body is floating with respect to the underlying substrate, the pass transistor is not electrically connected to ground potential". However, this argument is not persuasive because the limitation that the pass transistor is not electrically connected to ground potential is not recited in the claim.

With respect to applicant's argument that the modifying of the structure shown in Au to an SOI environment would destroy the operability of the device in Au because Au relies on the body being non-floating. However, this argument is not persuasive because there is no

indication in Au that the MOSFET Q1, Figure 4b cannot be constructed using SOI technology, and as discussed above, the MOSFET Q1 is reasonable to be fabricate by using SOI technology so the floating of the body of transistor Q1 (using SOI technology) does not destroy the operation of the circuitry since the body of Q1 is still being controlled by the network 40 (this is similar as applicant's invention that the body of the transistor is also controlled by a body control network).

Applicant also argues that the transferring of the structures shown in AU and Ker to an SOI environment (combine with Brady) would also render the operation of the devices in Au and Ker non-functional because Au and Ker rely upon the body being non-floating in order to have the devices properly operated. However, this argument is not persuasive because the body of each transistor in the modification/combination of Ker and Au is controlled by a body control network, and when the MOSFET transistors are fabricated by using SOI technology, the bodies of the transistors are still controlled by the body control network (this is also similar as applicant's invention that each of the bodies of the transistors is controlled by a body control network).

With regard to the Sasaki reference, applicant argues that "Sasaki teaches gate modulation and not body modulation". However, this argument is not persuasive because, as discussed in the above rejections, the Sasaki reference is used in the combination/modification to show the evidence that an ON MOSFET transistor functions as a resistor so that it is obvious to one skill in the art to use a MOSFET transistor that has its gate connected to a DC bias so that the transistor is always ON to implement a resistor for the purpose of easily integrated the circuitry and the circuitry is also fully integrated. Note that because the MOSFET transistors in the circuit are modified to be fabricated by using SOI technology as discussed in the

modification, so the MOSFET transistor that is used to implement the resistor is also an SOI MOSFET transistor.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

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LONG NGUYEN
PRIMARY EXAMINER